Lecture 4

Understanding op-amp models

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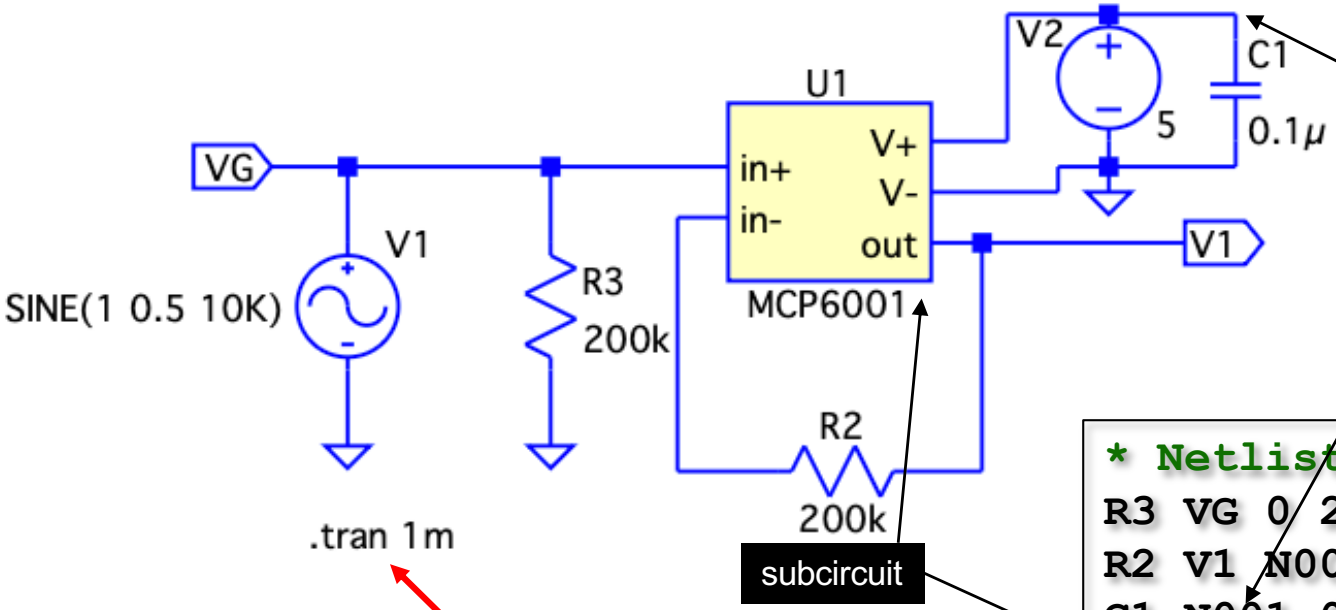
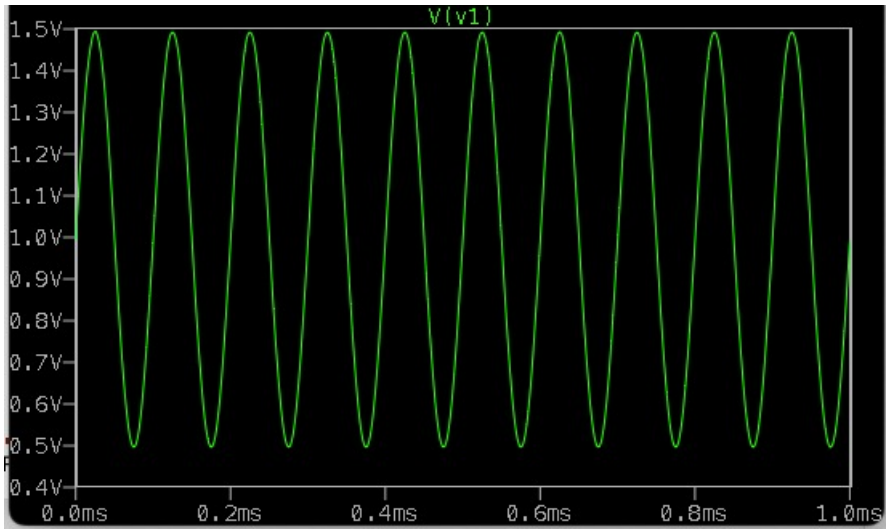
What is SPICE Simulator?

- Simulation Program with Integrated Circuit Emphasis
  - Developed by Larry Nagel at Berkeley in 1970's (under Prof Don Pederson).
  - Many commercial and freeware versions available.
  - Most significant CAD tool that drove the advancements in microelectronics.
- Linear Technology SPICE (LTspice)
  - Developed by Mike Engelhardt in early 2000s when he worked for Linear Technology (later bought by Analog Devices).
  - Added schematic capture and results plotting.
  - Engelhardt now has his own company marketing Qspice – not free.
- Input to SPICE is a SPICE netlist – multiple lines of text that describe:
  - Components and voltage/current sources in a circuit.
  - How the components and sources are connected to each other.
  - Model of components.
  - Type of analysis to be performed by the simulator

Example of a Spice netlist






```
* Netlist for Lab1Task2
R3 VG 0 200k
R2 V1 N002 200k
C1 N001 0 0.1µ
XU1 VG N002 N001 0 V1 MCP6001
V2 N001 0 5
V1 VG 0 SINE(1 0.5 10K)
.tran 1m
.lib /Volumes/External
SSD/Dropbox/_My
Documents/MCP6001.mod
.backanno
.end
```

SPICE Cheat Sheet

Letter	Component
R	Resistor
C	Capacitor
L	Inductor
V	independent voltage source
I	Independent current source
M	MOSFET
D	Diode
Q	Bipolar transistor
X	Subcircuit
E	Voltage-controlled voltage source
G	voltage-controlled current source

Letter	Unit	Multiplier
T, t	tera	10 E+12
G, g	giga	10 E+9
MEG, meg	mega	10 E+6
K, k	kilo	10 E+3
M, m	milli	10 E-3
U, u	micro	10 E-6
N, n	nano	10 E=9
P, p	pico	10 E-12

Directive	Action
.op	DC operating point analysis
.ac	Small signal AC analysis
.tran	Transient analysis
.backanno	Annotate current back to ports
.include	Include another file
.lib	Include a library
.end	End of netlist
.ends	End of subcircuit
.ic	Set initial condition

```
* Netlist for Lab1Task2
R3 VG 0 200k
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V2 N001 0 5
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.tran 1m
.lib /Volumes/External
SSD/Dropbox/_My Documents/MCP6001.mod
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.end
```
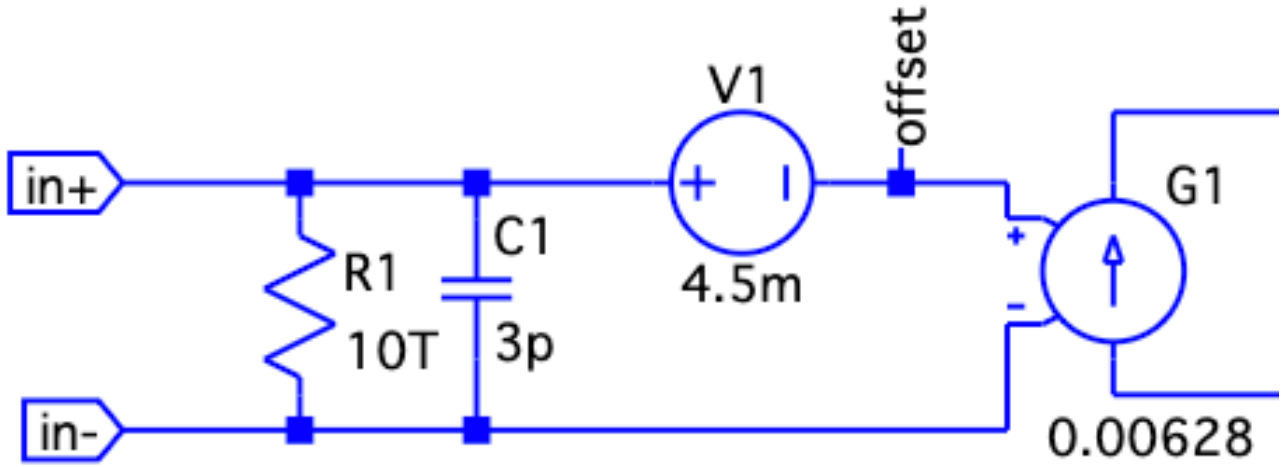
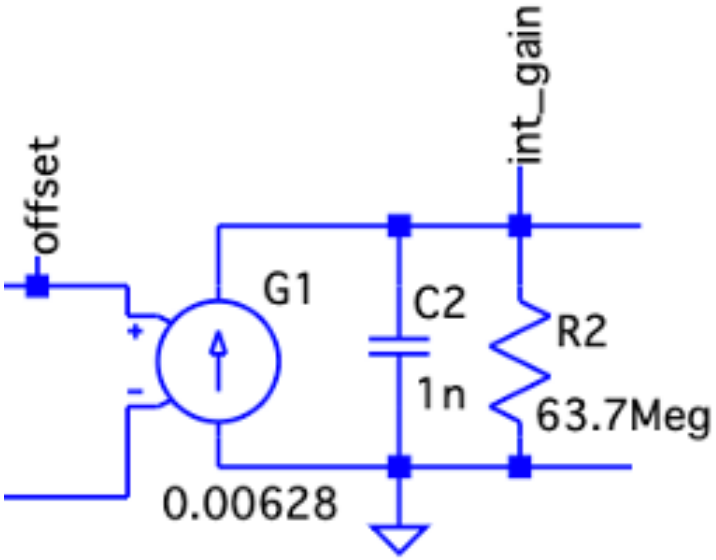

Model input stage of MCP6001

Differential Input Impedance	Z_{DIFF}	—	$10^{13}\|\|3$	—	Ω||pF
Input Offset Voltage	V_{OS}	-4.5	—	+4.5	mV




```
R1 in+ in- 10T
C1 in+ in- 3p
V1 in+ offset 4.5m
G1 0 int_gain offset in- 0.00628
```

Model gain vs frequency & slew rate of MCP6001



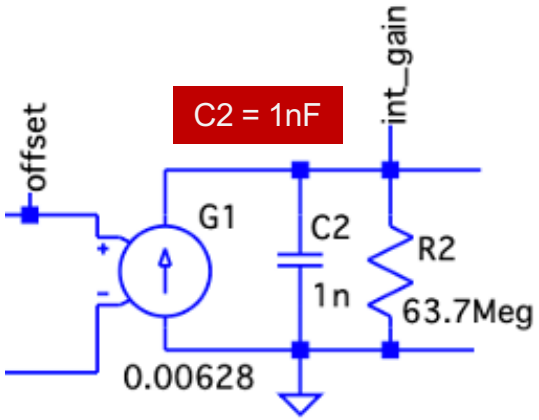

```
...
G1 0 int_gain offset in- 0.00628
R2 int_gain 0 63.7Meg
C2 int_gain 0 1n
```

- Assume compensation capacitor C2 is 1nF

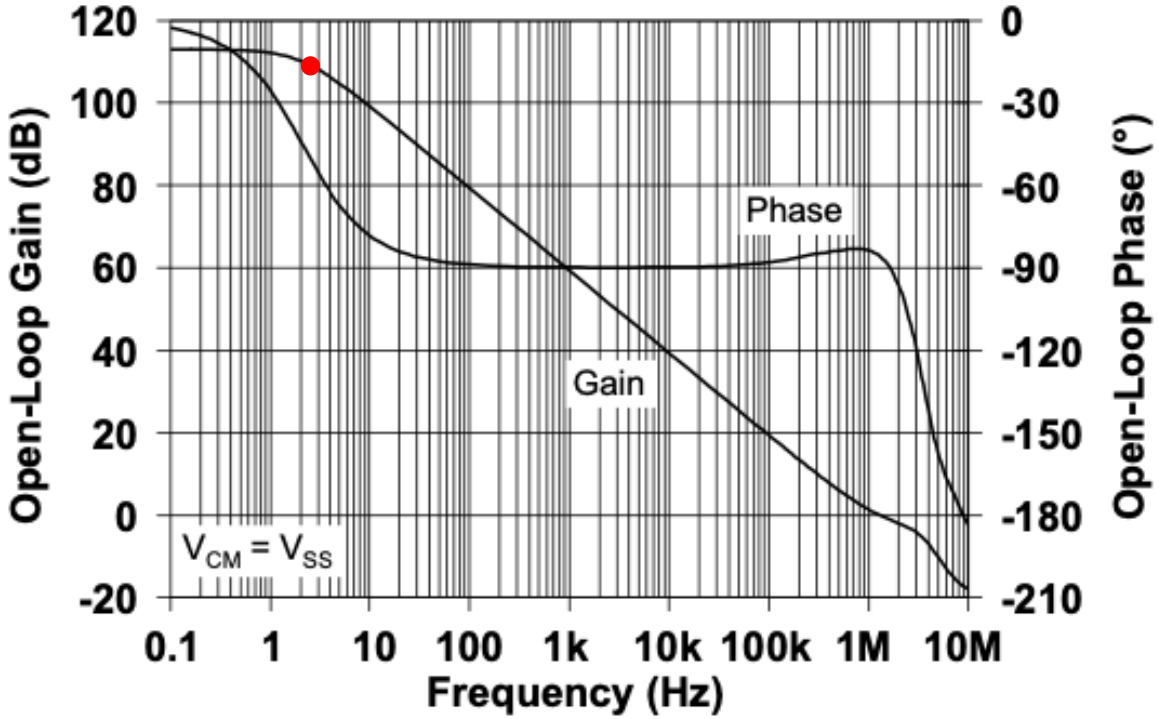
AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	G = +1 V/V
Slew Rate	SR	—	0.6	—	V/µs	

DC Open-Loop Gain (Large Signal)	A_{OL}	88	112	—	dB

Model open-loop gain vs frequency of MCP6001



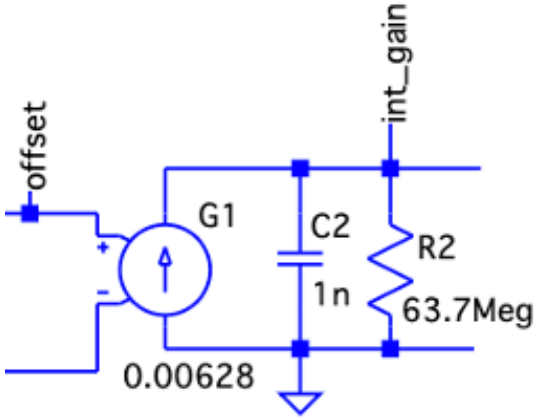

```
...
G1 0 int_gain offset in- 0.00628
R2 int_gain 0 63.7Meg
C2 int_gain 0 1n
```



- Dominant pole frequency $f_p = \frac{GBP}{A_{OL}} = \frac{10^6}{400000} = 2.5Hz = 1/2\pi R_2 C_2.$
- Therefore $R_2 = \mathbf{63.7{\times}10^6\Omega}$
- Calculate gm for G1:

$$gm{\times}R_2 = A_{OL}, \qquad \text{hence} \quad gm = \frac{400{,}000}{63.7}{\times}10^{-6} = \mathbf{0.00628}$$

Model Slew rate limit



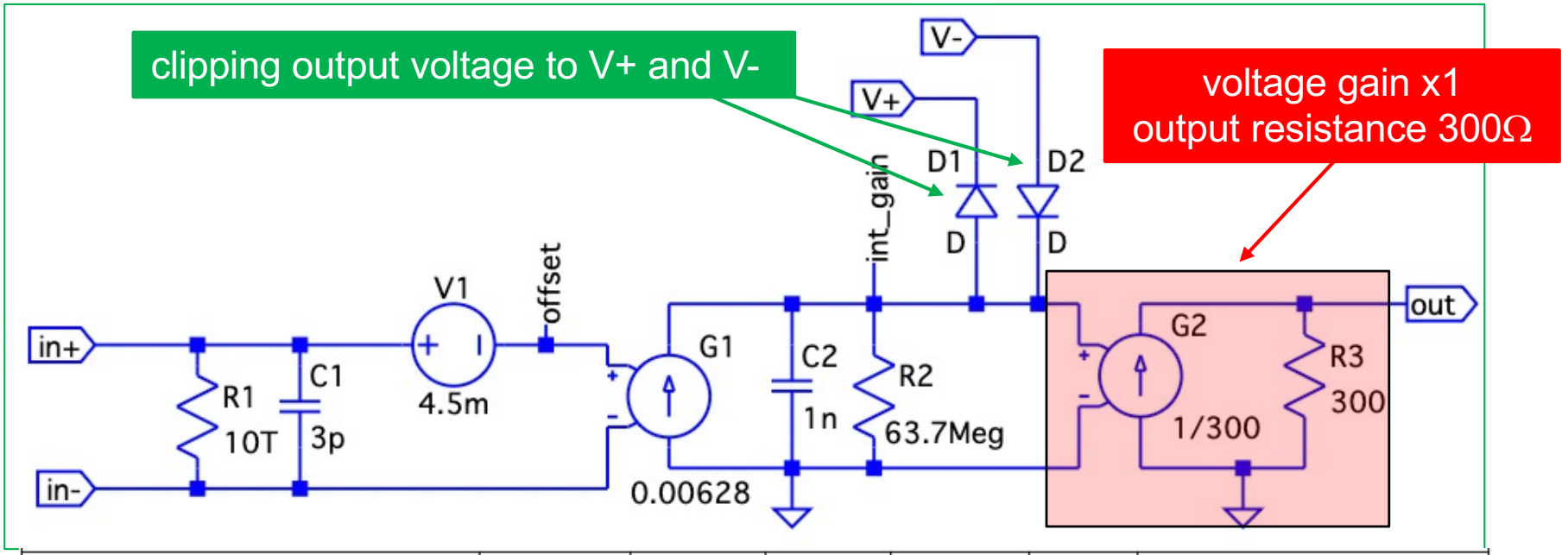
AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	G = +1 V/V
Slew Rate	SR	—	0.6	—	V/µs	

- Model the slew rate limit of 0.6V/us:

$$SR = max\frac{dV_{c2}}{dt} = \max(current\ of\ G1)\ /C2, \qquad \text{therefore}\ \ \max(current) = SR \times C_2 = 0.6mA$$

```
G1 0 int_gain value={limit(0.00628*V(offset,in-),0.6m, -0.6m)}
R2 int_gain 0 63.7Meg
C2 int_gain 0 1n
```

Model the output stage of MCP6001

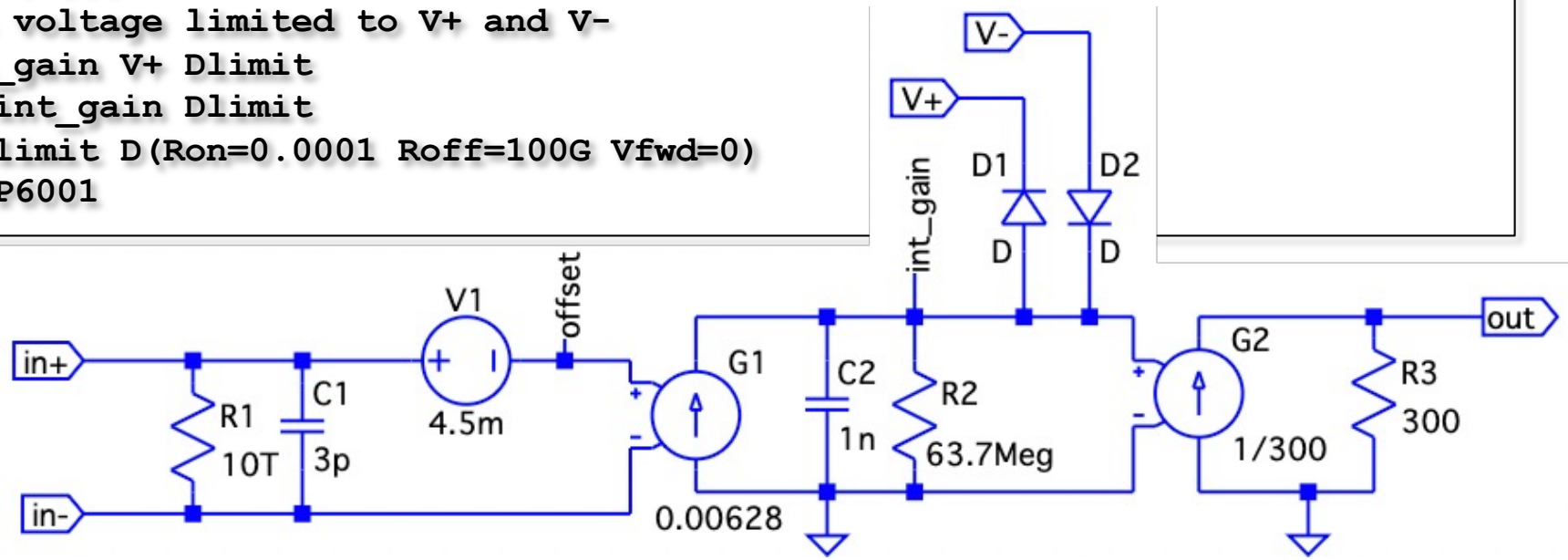


Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 5.5V, 0.5V input overdrive
Output Short-Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V

```
* output stage - current limit to +/- 20mA, ROUT = 300 ohm
G2 0 out value={limit(V(int_gain, 0)/300, 20m, -20m)}
R3 out 0 300
* output voltage limited to V+ and V-
D1 int_gain V+ Dlimit
D2 V- int_gain Dlimit
.model Dlimit D(Ron=0.0001 Roff=100G Vfwd=0)
```

The complete model of MCP6001

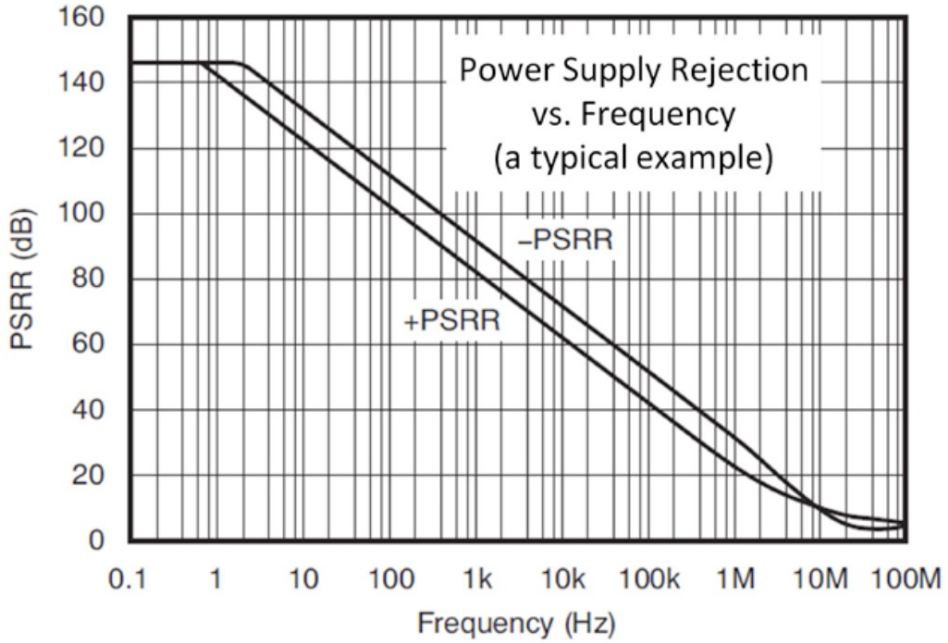
```
.subckt MCP6001 in+ in- V+ V- out
* input stage - RIN = 10T, CIN = 3p, Voffset = 4.5m
  R1 in+ in- 10T
  C1 in+ in- 3p
  Voffset in+ offset dc 4.5m
* gain stage - R2 = {AOL/(6.28*GBP*CPOLE)}, AOL = 400k, GBP = 1Meg, CPOLE = 1n
* gm = 6.28*GBP*CPOLE, current limit IMAX = +/- 0.6mA
  G1 0 int_gain value={limit(0.00628*V(offset,in-),0.6m, -0.6m)}
  R2 int_gain 0 63.7Meg
  C2 int_gain 0 1n
* output stage - current limit to +/- 20mA, ROUT = 300 ohm
  G2 0 out value={limit(V(int_gain, 0)/300, 20m, -20m)}
  R3 out 0 300
* output voltage limited to V+ and V-
  D1 int_gain V+ Dlimit
  D2 V- int_gain Dlimit
.model Dlimit D(Ron=0.0001 Roff=100G Vfwd=0)
.ends MCP6001
```

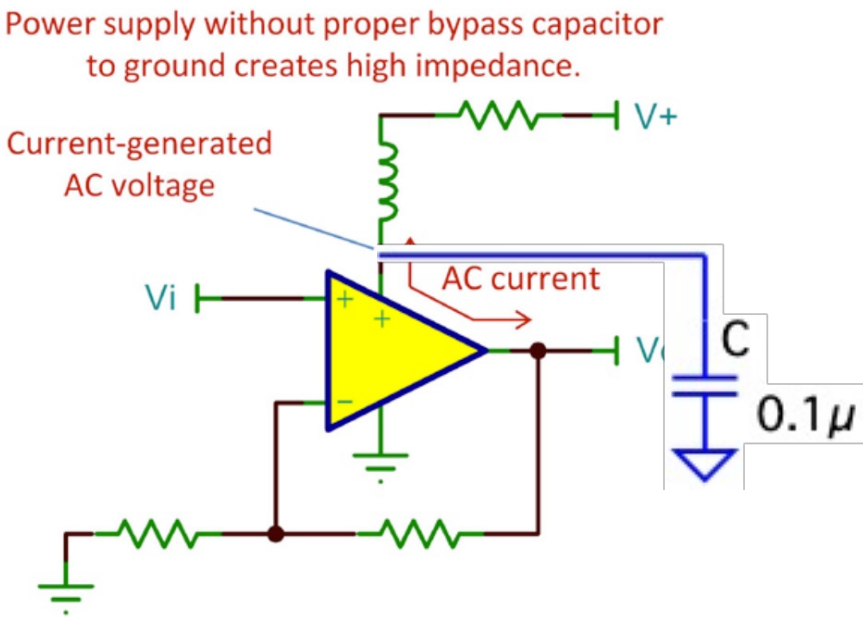


What specifications are NOT modelled?

- Common mode input impedances
- Common mode rejection ratio
- Power supply rejection ratio
- Common mode input voltage clipping
- Temperature effect on input bias current and offset voltage
- Noise characteristics of the op-amp
- Quiescent current of the op-amp

Power supply bypass (decoupling) capacitor





- Wire connection from power supply to op-amp power pin is an inductor.
- Inductor has high impedance at high frequency.
- Current draw through op-amp causes current fluctuation in inductor – can feedback to the op-amp.
- Resulting in op-amp prone to oscillation at high frequency or output overshoot.
- Add ceramic or tantalum capacitor close to op-amp supply pin to bypass (or decouple) any such high frequency fluctuations.